609, 610; 611, 612. The transistors 607-612 are coupled between a voltage source V and ground by the control transistor 606 and a transistor ~~614~~ 613 configured as a diode. This circuit uses a cross coupled connection between transistors 610, 611 to increase the gain of the circuit.

On page ~~15~~ 17, lines ~~13~~ 7 – ~~22~~ 21, please amend the paragraph as follows:

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Turning now to Figure 6B, a transistor level schematic for an exemplary embodiment of a selected portion of the digital filter 440 of Figure 4 is shown. The portion of the digital filter 440 illustrated in Figure 4B may be replicated four times with each replicated portion being coupled to one of the lines 431, 432, 433, 434 from the digital circuit 430 of Figure 4. The digital filter 440 includes four transistors 650, 651, 652, 653 serially connected between a voltage supply V and ground. The transistors 650, 653 are respectively a PMOS and an NMOS type transistor, and both have their bases coupled to receive a control signal, SAMPFILTER. The transistors 651, 652 are both NMOS type transistors with their bases respectively coupled to receive the last two temperature signals, ~~TEMP1~~ TEMP2 and ~~TEMP2~~ TEMP1 generated on the corresponding line 431, 432, 433, 434 from the logic circuit 430. The TEMP1 and TEMP2 signals may be derived from a pair of serially connected flip flops or latches (not shown) that are clocked at a frequency approximately twice the frequency associated with the SAMPFILTER signal. Thus, each time the SAMPFILTER signal transitions, the flip flops will have received and stored the last two temperature signals over, for example the line 431.

On page 18, lines 18 – 22, please amend the paragraph as follows:

Thus, those skilled in the art will appreciate that the illustrated circuitry requires two consecutive temperature signals, TEMP1 and TEMP2, to be logically "high" before the digital